PTO 06-4502

CY=JA DATE=19931214 KIND=B2
PN=05-086864

# READ WRITE METHOD FOR SEMICONDUCTOR DEVICE
[Handotai sochi ni okeru kakikomi, yomidashi hoho]

Kato Koichi

UNITED STATES PATENT AND TRADEMARK OFFICE
Washington, D.C. May 2006

Translated by: FLS, Inc.

| | | |
|---|---|---|
| PUBLICATION COUNTRY | (19): | JP |
| DOCUMENT NUMBER | (11): | 5-86864 |
| DOCUMENT KIND | (12): (13): | B2 |
| PUBLICATION DATE | (43): | 19870114 |
| PUBLICATION DATE | (44): | 19931214 |
| APPLICATION NUMBER | (21): | 60-114563 |
| APPLICATION DATE | (22): | 19850703 |
| ADDITION TO | (61): | |
| INTERNATIONAL CLASSIFICATION | (51): | H01L 27/108 |
| DOMESTIC CLASSIFICATION | (52): | |
| PRIORITY COUNTRY | (33): | |
| PRIORITY DATE | (32): | |
| PRIORITY NUMBER | (31): | |
| INVENTOR | (72): | KATO, KOICHI |
| APPLICANT | (71): | AGENCY OF IND SCIENCE & TECH |
| TITLE | (54): | READ WRITE METHOD FOR SEMICONDUCTOR DEVICE |
| FOREIGN TITLE | [54A]: | HANDOTAI SOCHI NI OKERU KAKIKOMI, YOMIDASHI HOHO |

(57) Claims

(1) A read write method for a semiconductor device, wherein a MOS transistor comprises a source-drain formed consisting of reverse-conductive impurities on both ends of an electrically floating conductive semiconductor layer and a gate electrode formed on the semiconductor layer via an insulating film, wherein during writing the applied voltage is reduced to zero in the gate voltage to drain voltage sequence or drain voltage to gate voltage sequence based on the data to be written after gate voltage exceeding the threshold value of the transistor and drain voltage generating impact ionization have been applied to write in an excessively low state with a sufficiently large number of carriers in the semiconductor layer, and wherein during reading gate voltage exceeding the threshold value of the transistor and drain voltage not generating impact ionization are applied to read the two types of written data.

(2) The method described in Claim 1, wherein the semiconductor layer forming the MOS transistor is formed on an insulator.

Detailed Description of the Invention

(Industrial Field of Application)

The present invention relates to a semiconductor memory device and, more specifically, to a read write method for a semiconductor device using a MOS transistor formed in a semiconductor layer on an insulator.

(Prior Art and Problem to be Solved)

It is commonly known, the elements formed in semiconductor layers have been miniaturized to significantly increase integration and processing speeds. However, the limits to miniaturization have been reached. The memory elements in dynamic memory consist of a single MOS transistor and single MOS capacitor. The capacity of capacitors has reached its limit, and it would be nearly impossible to improve integration given manufacturing limitations.

(Purpose of the Invention)

In light of this situation, the purpose of the present invention is to provide a read write method for semiconductor devices in which integration and high-speed processing can be obtained by realizing a smaller dynamic memory element configuration in a MOS transistor formed on top of an insulator.

(Summary of the Invention)

The framework of the present invention realizes a single memory element consisting of a single MOS transistor. By dynamically controlling the size of the voltage applied to the gate and drain of a MOS transistor formed on top of an insulator, the MOS transistor itself can perform memory functions.

In other words, the present invention is a read write method for a semiconductor device, wherein a MOS transistor comprises a source-drain formed consisting of reverse-conductive impurities on both ends of an electrically floating conductive semiconductor layer and a gate electrode formed on the semiconductor layer via an insulating film,

wherein during writing the applied voltage is reduced to zero in the gate voltage to drain voltage sequence or drain voltage to gate voltage sequence based on the data to be written after gate voltage exceeding the threshold value of the transistor and drain voltage generating impact ionization have been applied to write in an excessively low state with a sufficiently large number of carriers in the semiconductor layer, and wherein during reading gate voltage exceeding the threshold value of the transistor and drain voltage not generating impact ionization are applied to read the two types of written data.

(Effect of the Invention)

Because the present invention is a single memory element consisting of a single MOS transistor, the amount of space taken up by the element is reduced. Because it is a single memory element consisting of a single MOS transistor, the structure is simple and easy to manufacture.

(Working Examples of the Invention)

The following is a detailed explanation of the invention with reference to the working example in the drawings.

FIG 1 is a simplified diagram of the semiconductor device in a working example of the present invention. Here, a P-type silicon layer [21] formed on top of an insulator [10] is doped with N-type impurities to form source and drain regions [22, 23]. A gate electrode [25] is formed via a gate oxide film [24] to complete a channel-length 1.2 μm N-type MOS transistor [20]. The silicon film

[21] is created by forming a polycrystalline or amorphous silicon film such as an $SiO_2$ film on an insulator [10] and then beam annealing the silicon film to monocrystallize it. The monocrystallized silicon layer is oxidized except for the element formation regions to create an oxide film for element separation.

The source [22] in the MOS transistor [20] is grounded, and the drain [23] and source [25] are connected to the sense circuit [30]. Because the sense circuit [30] reads and writes the data stored in the MOS transistor [20], the size of the voltage applied to the gate and drain is dynamically controlled.

The sense circuit [30] has two modes of dynamic application during the data writing operation. In the first mode, as shown in FIG 2a, voltage approximating the threshold voltage (5 V) is applied to both the source and drain, the gate voltage **G** is reduced to zero, and the drain voltage **D** is then reduced to zero after 100 psec. In the second mode, as shown in FIG 2b, the drain voltage **D** is reduced to zero and the gate voltage **G** is then reduced to zero after 100 psec. During the data reading operation, voltage approximating the impact ionization voltage (2.5 V) is applied to the drain, and voltage approximating the threshold voltage is applied to the gate. The data written to the MOS transistor [20] is read from the current at this time.

As in a conventional semiconductor memory element, the MOS transistor [20] is arranged on a matrix, and the gate and drain are

connected by a word line and bit line to function as a memory circuit.

The following is an explanation of the operation of a device with this configuration.

First, the source voltage of the MOS transistor [20] is reduced to zero, and approximately 5 V is applied to the gate and drain. At this time, as shown in FIG 3a, the concentration of electrons forming the channel is high, holes are driven to the bottom of the silicon layer [21] and the absolute amount is reduced. Because the drain voltage is high, the holes generated by impact ionization near the drain are rebonded near the source.

When the gate voltage is reduced to 0 V, the substrate potential of the silicon layer [21] is sharply reduced and, as shown in FIG 3b, the electrons forming the channel, flow abruptly in the direction of the drain. Severe impact ionization occurs in the joined region near the drain at this time, and the generated holes are stored in the silicon layer [21]. After the gate voltage has been reduced to 0 V, the drain voltage is reduced to 0 V after 100 psec, and the state returns to near equilibrium.

In the state shown in FIG 3a, by contrast, when the drain voltage is reduced to 0 V and the gate voltage is reduced to 0 V after 100 psec, the electrons forming the channel as shown in FIG 3c flow in both directions with respect to the source and drain. However, because both the source and drain are at 0 V, the potential gradient is small and hardly any impact ionization occurs. In a

silicon layer with the electrons flowing out, the holes are in a slight state of disequilibrium.

By selecting one of two directions, sufficient or insufficient holes stored in the silicon layer, a MOS transistor [20] can function as a memory element.

During the reading operation, a drain voltage causing no impact ionization is applied. When threshold gate voltage is applied with the silicon layer [21] in a near equilibrium state (see FIG 3b), the amount of holes in the silicon layer [21] is high as shown in FIG 4a, and the drain current flows due to the overshoot. In contrast, if the same voltage is applied when the silicon layer [21] is in a disequilibrium state (see FIG 3c) as shown in FIG 4b, the substrate potential is low and the drain current hardly flows at all because the amount of holes is low.

Therefore, two types of data can be detected based on whether or not there are a sufficient amount of holes in the silicon layer [21].

In this working example, the MOS transistor [20] functioned as a memory element. In other words, a memory cell was created from a single MOS transistor [20]. Compared to memory cells of the prior art consisting of a single transistor and single capacitor, this memory cell allows for greater integration and faster processing speeds. Because the element structure is simple, it is easy to manufacture.

The present invention is by no means restricted to this working example. For example, the MOS transistor does not have to be an N-type transistor. It can be a P-type transistor as well. Also the

silicon layer does not have to be formed on an amorphous insulator (SOI) such as $SiO_2$. For example, it can be a layer (SOS) formed on a sapphire monocrystalline insulator. In addition, the bias conditions for applying voltage to the gate and drain of the MOS transistor can be adjusted depending on the physical properties of the MOS transistor being used. In other words, other variations are possible within the scope of the present invention.

Brief Explanation of the Drawings

FIG 1 is a simplified diagram of the semiconductor device in a working example of the present invention. FIG 2 a, b are signal diagrams used to explain the operation of the sense circuit used in the same device. FIG 3 a-c are diagrams used to explain the writing operation. FIG 4 a, b are diagrams used to explain the reading operation.

10 ... insulator, 20 ... N-channel MOS transistor, 21 ... P-type silicon layer, 22 ... source, 23 ... drain, 24 ... gate oxide film, 25 ... gate electrode, 30 ... sense circuit

FIG 1

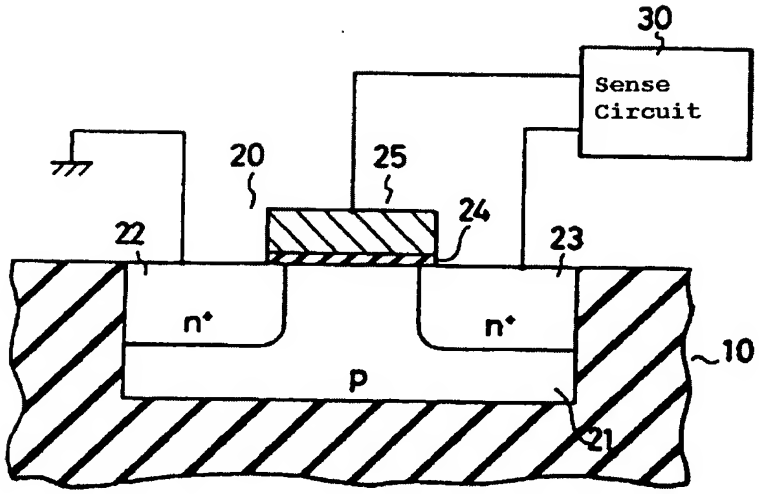


FIG 2

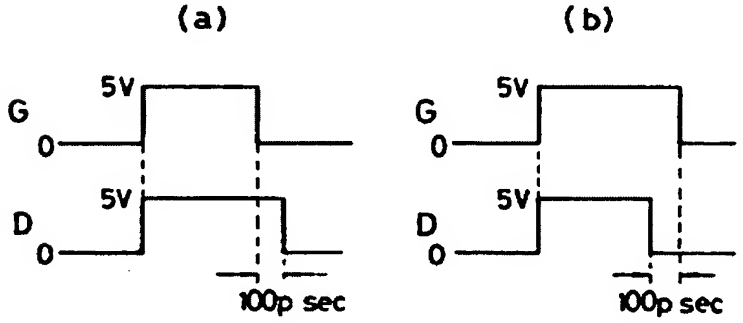

FIG 3

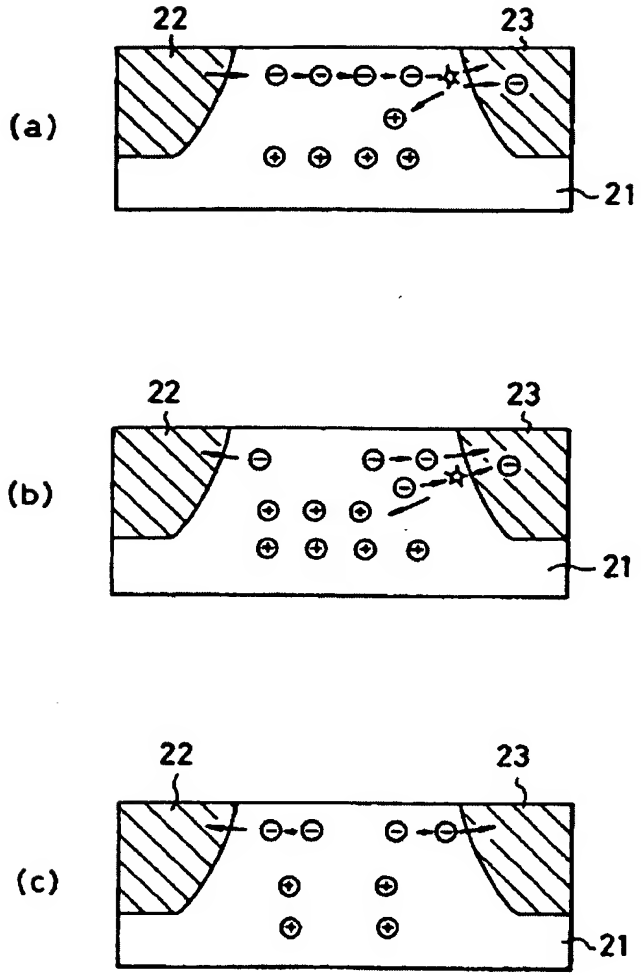

FIG 4